REMARKS

The Office Action mailed May 6, 2004 has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

No extension of time is believed to be required based upon the filing of this Amendment prior to the deadline of the three-month statutory period (i.e., August 6, 2004). Authorization is granted to charge counsel's Deposit Account No. 01-2300, referencing **Attorney Docket No. 024016-00020**, for any additional fees necessary for entry of this Amendment.

As a preliminary matter, Applicant appreciates the indication that claims 4, 12-16 and 21-27, objected to as being dependent upon a rejected base claim, would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Applicant, however, respectfully submits that all of the presently pending claims recite allowable subject matter and therefore placing claims 4, 12-16 and 21-27 into independent form is believed to be unnecessary.

The Abstract has been amended. It is submitted that the amendments made herein are fully supported in the Specification and the drawings, as originally filed, and therefore no new matter has been introduced. Accordingly, claims 1-28 are pending in the present application and are respectfully submitted for reconsideration.

The Abstract stands objected to for an informality. The Abstract has been amended in response to the Examiner's objection, and it is submitted that the Abstract, as amended, complies with 37 C.F.R. § 1.72(b). The objection is respectfully traversed and reconsideration is requested.

Independent claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's prior art in view of the Carson et al. patent (U.S. Patent No. 6,125,158). The rejection is respectfully traversed and reconsideration is requested.

Independent claim 1 recites a PLL frequency synthesizer, comprising a voltage-controlled oscillator for outputting an output frequency signal corresponding to a control voltage signal; a phase comparator for outputting an output signal corresponding to a phase comparison between the output frequency signal and a reference frequency signal; and a charge pump circuit for varying the control voltage signal according to the phase-compared signal; whereby a feedback loop is configured, wherein signal flow of the feedback loop is periodically varied in a phase comparison cycle used in the phase comparator. Applicant respectfully submits that the Applicant's prior art in view of the Carson et al. patent do not disclose or suggest the PLL frequency synthesizer, as claimed in the present invention.

As acknowledged by the Examiner, the Applicant's prior art "fails to teach a signal flow of the feedback loop is periodically varied in a phase comparison cycle used in the phase comparator." The Examiner proceeds to rely on the Carson et al. patent as disclosing such signal flow. The Carson et al. patent, however, merely discloses a PLL circuit which comprises a plurality of comparator, namely, a fine comparator and coarse comparator, wherein the coarse comparator conducts normal phase comparison operation and the fine comparator compares phase of a clock signal through a delay circuit. Specifically, the PLL circuits disclosed in the Carson et al. patent do not have a switch control circuit for transmitting phase correction pulses outputted from a phase comparator to a charge pump while being locked, and operation while being locked is similar to a typical PLL circuit. More specifically, the cited reference fails to disclose restraining propagation of pseudo correction pulses that occur every cycle of the

reference frequency signal (f_{in}) while being locked. In contrast, the present invention relates to a PLL frequency synthesizer, and particularly to a PLL frequency synthesizer capable of achieving an improvement in spurious characteristic in a steady state while maintaining a high-speed lockup characteristic. In the present invention, the signal flow of the feedback loop can be varied during the period in which the pseudo correction pulse is outputted from the charge pump circuit for each phase comparison period or cycle of the phase comparator. Therefore, the characteristic of response of the voltage-controlled oscillator to the pseudo correction pulse outputted from the charge pump circuit can be controlled while the signal flow of the feedback loop in the steady operating state other than the pseudo correction pulse output period set for each phase comparison cycle is being maintained. Further, spurious generation that occurs due to the pseudo correction pulse can be suppressed in the steady operation state of the PLL frequency synthesizer. Accordingly, the Carson et al. patent also does not disclose or suggest that a signal flow of the feedback loop is periodically varied in a phase comparison cycle used in the phase comparator, as claimed.

Since neither the Applicant's prior art nor the Carson et al. patent discloses the PLL frequency synthesizer, as claimed, Applicant submits that even if the references were combinable, as suggested, such alleged combination clearly does not disclose or suggest the present invention, as claimed. Nor even if the references were combinable would such alleged combination result in the claimed invention. It is therefore submitted that neither reference, alone or in alleged combination, discloses or suggests the PLL frequency synthesizer, as claimed, particularly, a PLL frequency synthesizer wherein a signal flow of the feedback loop is periodically varied in a phase comparison cycle used in the phase comparator. Based upon the

above. Applicant respectfully submits that independent claim 1 is patentable and in condition for allowance. Reconsideration is respectfully requested.

Dependent claims 2-3 and 7-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's prior art in view of the Carson et al. patent and further in view of the Bortolini et al. patent (U.S. Patent No. 5,473,640). Dependent claims 5-6 and 9-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's prior art in view of the Carson et al. patent, the Bortolini et al. patent and further in view of the Weindorf patent (U.S. Patent No. 6,396,217). Dependent claims 11 and 17-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's prior art in view of the Carson et al. patent and further in view of the Abe et al. patent (U.S. Patent No. 5,794,130). Dependent claims 19-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's prior art in view of the Carson et al. patent, the Abe et al. patent and further in view of the Weindorf patent. Dependent claims 28 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's prior art in view of the Carson et al. patent, the Abe et al. patent and further in view of the Mole et al. patent (U.S. Patent No. 6,226,509). The rejections are respectfully traversed and reconsideration is requested.

With respect to the rejections of the dependent claims and the further secondary references cited by the Examiner, the Bortolini et al. patent is directed to a PLL circuit in which the PLL circuit is initialized immediately after power-up in accordance with a memory in a processor and calibration is conducted so as to shorten lock draw time immediately after the power-up. The Weindorf patent is directed to light intensity offset error lowering method for a display lightness control device which has a circuit for dividing voltage of DAC output. The Abe et al. patent is directed to a PLL circuit in which post-lock time, until the PLL circuit is

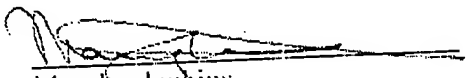
locked, is shortened by changing a time constant of a filter circuit (LPF) to a time constant smaller by length of predetermined time at the time of power-on. With reference to Fig. 4, the Mole et al. patent is directed to an image rejection mixer for converting frequency in which RC poly-phase filters (R1, C1-R4, C4) are arranged between transistors (Q1 through Q4) for lower input stage and transistors (Q5 through Q12) for upper mixer stage, thereby to reject image frequency components.

With reference to the above arguments concerning independent claim 1, Applicant further submits that the Applicant's prior art, the Carson et al. patent, the Bortolini et al. patent, the Weindorf patent, the Abe et al. patent and the Mole et al. patent, either alone or in the alleged combinations suggested by the Examiner in the Office Action, do not disclose or suggest the content of dependent claims 2-3, 5-11, 17-20 and 28, which depend from independent claim 1. Specifically, the PLL circuits disclosed in the Bortolini et al. patent and the Abe et al. patent also do not have a switch control circuit for transmitting phase correction pulses outputted from a phase comparator to a charge pump while being locked, and operation while being locked is similar to a typically PLL circuit. Moreover, the cited references also fail to disclose restraining propagation of pseudo correction pulses that occur every cycle of reference signal (f_{in}) while being locked. Further, the Weindorf patent and the Mole et al. patent are not directed to PLL circuits. Thus, the Bortolini et al. patent, the Weindorf patent, the Abe et al. patent and the Mole et al. patent, either alone or in the alleged combinations suggested by the Examiner, also do not disclose or suggest the PLL frequency synthesizer, as claimed. Moreover, there is no suggestion to combine the references, as suggested by the Examiner in the Office Action. Applicant therefore submits that the dependent claims are also patentable and in condition for allowance. Reconsideration is requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned counsel at the telephone number, indicated below, to arrange for an interview to expedite the disposition of this application.

Dated: August 5, 2004

Respectfully submitted,



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